**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings of claims in the application:

**Listing of Claims:**

Claims 1-24 (canceled)

Claim 25 (previously presented) A serial-to-parallel data conversion circuit comprising:

a first shift register coupled to receive serial data;

a second shift register coupled to receive parallel data bytes from the first shift register in response to a first periodic signal; and

a third shift register coupled to receive the parallel data bytes from the second shift register,

wherein the first periodic signal causes boundaries between the parallel data bytes in the second shift register to change in response to a second signal.

Claim 26 (previously presented) The serial-to-parallel data conversion circuit defined in claim 25 further comprising:

a first counter circuit that generates the first periodic signal and that causes a period of the first periodic signal to increase in response to the second signal.

Claim 27 (previously presented) The serial-to-parallel data conversion circuit defined in claim 26 further comprising:

a second counter circuit generating a second periodic signal that causes the third shift register to receive the parallel data bytes from the second shift register.

Claim 28 (previously presented) The serial-to-parallel data conversion circuit defined in claim 27 further comprising:

a phase locked loop circuit that generates a clock signal, the clock signal shifting the data through the first shift register.

Claim 29 (currently amended) The serial-to-parallel data conversion circuit defined in claim 28 further comprising:

a fourth shift register coupled to the first counter and the second shift register, the fourth register synchronizing the first periodic signal to the clock signal; and

a fifth shift register coupled to the second counter circuit and the third shift register, the fifth register synchronizing the second periodic signal to the clock signal.

Claim 30 (previously presented) The serial-to-parallel data conversion circuit defined in claim 29 wherein the second counter circuit also generates a third periodic signal that controls circuitry receiving the parallel data bytes from the third shift register.

Claim 31 (previously presented) The serial-to-parallel data conversion circuit defined in claim 25 wherein the serial-to-parallel data conversion circuit is embedded on an FPGA.

Claim 32 (previously presented) A serial-to-parallel data conversion circuit comprising:

a first data storage circuit coupled to receive serial data;

a second data storage circuit coupled to receive parallel data bytes from the first data storage circuit in response to a first periodic signal; and

a first control circuit generating the first periodic signal that causes boundaries between each of the parallel data bytes received in the second data storage circuit to change in response to a second signal; and

a third data storage circuit coupled to receive the parallel data bytes from the second data storage circuit.

Claim 33 (previously presented) The serial-to-parallel data conversion circuit defined in claim 32 further comprising:

a second control circuit generating a second periodic signal that causes the third data storage circuit to receive the parallel data bytes from the second data storage circuit.

Claim 34 (previously presented) The serial-to-parallel data conversion circuit defined in claim 32 wherein the first control circuit causes a period of the first periodic signal to increase in response to a pulse in the second signal, and each pulse in the second signal causes the boundaries between each of the parallel data bytes to change by one bit.

Claim 35 (previously presented) The serial-to-parallel data conversion circuit defined in claim 34 wherein one bit stored in the first data storage circuit is lost after each pulse in the second signal.

Claim 36 (previously presented) The serial-to-parallel data conversion circuit defined in claim 33 further comprising:

a phase locked loop circuit generating a clock signal that controls shifting of bits through the first data storage circuit.

Claim 37 (previously presented) The serial-to-parallel data conversion circuit defined in claim 36 further comprising:

a first register that eliminates skew between the first periodic signal and the clock signal; and

a second register that eliminates skew between the second periodic signal and the clock signal.

Claim 38 (previously presented) The serial-to-parallel data conversion circuit defined in claim 32 further comprising:

a logic gate that prevents the second signal from changing boundaries of the parallel data bytes in response to a third signal.

Claim 39 (previously presented) The serial-to-parallel data conversion circuit defined in claim 32 wherein the serial-to-parallel data conversion circuit is embedded in a PLD.

Claim 40 (previously presented) The serial-to-parallel data conversion circuit defined in claim 39 wherein the second signal is driven from a state machine on the PLD.

Claim 41 (previously presented) The serial-to-parallel data conversion circuit defined in claim 39 wherein the second signal is driven from an input/output pin of the PLD